AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY PRESENTED) An apparatus comprising:

an AND plane configured to generate a product term in response to a plurality of product term inputs; and

a plurality of product term input circuits each configured (i) to receive an input signal and (ii) to generate one of said plurality of product term inputs, wherein each of said plurality of product term input circuits comprises (i) a first memory cell directly connected to an input terminal of a first transmission gate and (ii) a second memory cell directly connected to an input terminal of a second transmission gate, wherein (i) an output terminal of said first transmission gate is connected to an output terminal of said second transmission gate, (ii) said input signal is presented to a first control terminal of said first transmission gate and a first control terminal of said second transmission gate and (iii) said product term input is configurable in response to contents of said first memory cell and said second memory cell to present either (i) a signal that varies in response to said input signal or (ii) a predetermined logic level that is independent of said input signal.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein each of said first transmission gate and said second transmission gate further comprise a second control terminal configured to receive a complement of said input signal.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first memory cell and said second memory cell comprise a first configuration bit and a second configuration bit, respectively, of said apparatus.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said output terminal of said first transmission gate and said output terminal of said second transmission gate are connected to an input of said AND plane.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said input signal comprises an input term.

6. (CURRENTLY AMENDED) An apparatus comprising:

an AND plane configured to generate a product term in response to a plurality of product term inputs;

a first circuit configured to present a first value stored in a first memory cell as one of said plurality of product term inputs in response to a first state of an input signal; and

a second circuit configured to present a second value stored in a second memory cell as said one of said plurality of product term inputs in response to a second state of said input signal, wherein (i) said first and said second stored values are programmable during configuration of said apparatus and (ii) said product term input is programmable as any of (i) said input signal, (ii) a digital complement of said input signal, and (iii) a predetermined logic level.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein:

said first circuit comprises a first transmission gate configured to couple said first memory cell to an input terminal of said AND plane;

said second circuit comprises a second transmission gate configured to couple said second memory cell to said input terminal of said AND plane; and

said input signal is coupled to a control terminal of said first and said second transmission gates.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein each of said first transmission gate and said second transmission gate comprise a CMOS transistor pair.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein:

said first circuit further comprises a first CMOS inverter coupling said first memory cell to said first transmission gate; and

said second circuit further comprises a second CMOS inverter coupling said second memory cell to said second transmission gate.

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said product term input comprises (i) a predetermined logic level when said first and said second memory cells contain the same data and (ii) a signal that varies in response to said input signal when said first and said second memory cells contain different data.

11. (ORIGINAL) The apparatus according to claim 10, wherein said data comprises configuration bits.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said first memory cell and said second memory cell are configured to source and sink a current.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said apparatus comprises a programmable logic device.

14. (PREVIOUSLY PRESENTED) The apparatus according to claim 6 further comprising:

a group of gates configured to generate a sum-of-products term in response to a plurality of product terms, wherein said AND plane is further configured to generate said plurality of product terms.

15. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said input signal comprises an input term.

16. (CURRENTLY AMENDED) The ~~apparatus~~ method according to claim ~~15~~ 18, wherein said product term input is programmable as any of (i) said input ~~term~~ signal, (ii) a digital complement of said input ~~term~~ signal, and (iii) a predetermined logic level.

17. (CURRENTLY AMENDED) The apparatus according to claim ~~16~~ 6, wherein said predetermined logic level is selectable from a digital 0 and a digital 1.

18. (PREVIOUSLY PRESENTED) A method for providing a product term input of a programmable logic device comprising the steps of:

(A) presenting a first value stored in a first memory cell to an input node of an AND plane via a first transmission gate in response to a first state of an input signal; and

(B) presenting a second value stored in a second memory cell to said input node of said AND plane via a second transmission gate in response to a second state of said input signal, wherein said first and said second stored values are programmed during configuration of said programmable logic device.

19. (PREVIOUSLY PRESENTED) The method according to claim 18, wherein said input signal comprises an input term of a logic block of said programmable logic device.

20. (PREVIOUSLY PRESENTED) The method according to claim 18, further comprising the steps of:

(C) generating a first logic level at said input node in response to said first and said second stored values being programmed with a first value;

(D) generating a second logic level at said input node in response to said first and said second stored values being programmed with a second value;

(E) generating a signal at said input node that has a state similar to said input signal in response to said first stored value being programmed with said first value and said second stored value being programmed with said second value; and

(F) generating a signal at said input node that has a state similar to a digital complement of said input signal in response to said first stored value being programmed with said second value and said second stored value being programmed with said first value.